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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0756-1838

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title: SEMICONDUCTOR DEVICE, METHOD OF FABRICATING SAME, AND, ELECTROOPTICAL DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [15]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [3]
4. [X] Oath or Declaration *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed)
      [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    [X] Divisional of prior application Serial No. 08/962,840, filed November 3, 1997; which itself is a continuation of Serial No. 08/575,355, filed December 20, 1995, now abandoned.
    Prior application information: Examiner: R. Booth Group/Art Unit: 1107

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label or [X] Correspondence address below

(Insert Customer No. or Attach bar code label here)

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Name: Gerald J. Ferguson, Jr. Registration No. 23,016

Signature Date: July 17, 1998

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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12

TOTAL AMOUNT OF PAYMENT	($)790.00

Complete If Known	
Application Number	
Filing Date	July 16, 1998
First Named Inventor	Shunpei YAMAZAKI et al.
Examiner Name	R. Booth
Group Art Unit	1107
Attorney Docket Number	0756-1838

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:
   Deposit Account No. 19-2380
   Deposit Account Name: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, PC

   [X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

   [ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [X] Payment Enclosed:
   [X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	[ ]
107	540	207	270	Plant filing fee	[ ]
108	790	208	395	Reissue filing fee	[ ]
114	150	214	75	Provisional filing fee	[ ]

SUBTOTAL (1) $790.00

2. EXTRA CLAIM FEES

		Extra Claims	Fee from Below	Fee Paid
Total Claims	10 - 20** =	0	X _____ =	
Independent Claims	3 - 3** =	0	X _____ =	
Multiple Dependent Claims			_____ =	

**or number previously paid, if greater. For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) - 0 -

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Ext for reply within first month	
116	400	216	200	Ext for reply within second mth	
117	950	217	475	Ext for reply within third mth	
118	1,510	218	755	Ext for reply within fourth mth	
128	2,060	228	1,030	Ext for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing brief in support of appeal	
121	270	221	135	Request for Oral Hearing	
138	1,510	138	1,510	Petition to institute public use proceeding	
140	110	240	55	Petition to revive-unavoidable	
141	1,320	241	660	Petition to revive-unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of IDS	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	
				Other _____	
				Other _____	

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $ _____

SUBMITTED BY

Complete (if applicable)

Typed or Printed Name	Gerald J. Ferguson, Jr.			Reg. Number	23,016
Signature		Date	July 17, 1998	Deposit Account User ID	19-2380

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Patent Application of	)	
Shunpei YAMAZAKI et al.	)	
Based On Serial No. 08/962,840	)	Art Unit: 1107
Which Was Filed: November 3, 1997	)	Examiner: R. Booth
For: SEMICONDUCTOR DEVICE, METHOD OF FABRICATING SAME, AND, ELECTROOPTICAL DEVICE	)	Date: July 17, 1998

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Serial No. 08/962,840, filed November 3, 1997; which itself is a continuation of Serial No. 08/575,355, now abandoned.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

Gerald J. Ferguson, Jr.
Registration No. 23,016

Sixbey, Friedman, Leedom & Ferguson, P.C.
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TITLE OF THE INVENTION

Semiconductor Device, Method of Fabricating Same, and, Electrooptical Device

BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to a configuration of thin-film transistors (TFTs) formed on a flexible substrate (i.e., having mechanical flexibility) such as a resinous substrate which can be made of engineering plastics. The invention also relates to a method of fabricating such thin-film transistors. Furthermore, the invention relates to an active matrix liquid crystal display fabricated, using these thin-film transistors.

[Prior Art]

Thin-film transistors formed on glass substrates or on quartz substrates are known. Thin-film transistors formed on glass substrates are chiefly used in active matrix liquid crystal displays. Since active matrix liquid crystal displays can display images with high response and with high information content, it is expected that they can supplant simple matrix liquid crystal displays.

In an active matrix liquid crystal display, one or more thin-film transistors are disposed as a switching element at each pixel. Electric charge going in and out of the pixel electrode is controlled by this thin-film transistor. The substrates are made of glass or quartz, because it is necessary that visible light pass through the liquid crystal display.

Liquid crystal displays are display means which are expected to find quite extensive application. For example, they are expected to be used as display means for card-type computers, portable computers, and portable electronic

devices for various telecommunication appliances. As more sophisticated information is treated, more sophisticated information is required to be displayed on the display means used for these portable electronic devices. For example, there is a demand for functions of displaying higher information content and moving pictures as well as numerals and symbols.

Where a liquid crystal display is required to have a function of displaying higher information content and moving pictures, it is necessary to utilize an active matrix liquid crystal display. However, where substrates made of glass or quartz are used, various problems take place: (1) limitations are imposed on thinning of the liquid crystal display itself; (2) the weight is increased; (3) if the thickness is reduced in an attempt to reduce the weight, the substrate breaks; and (4) the substrate lacks flexibility.

Especially, card-type electronic devices are required to be so flexible that they are not damaged if slight stress is exerted on them when they are treated. Therefore, liquid crystal displays incorporated in these electronic devices are similarly required to be flexible.

The invention disclosed herein provides an active matrix liquid crystal display having flexibility.

SUMMARY OF THE INVENTION

One available method of imparting flexibility to a liquid crystal display is to use plastic or resinous substrates which transmit light. However, because of poor heat resistance of resinous substrates, it is technically difficult to form thin-film transistors on them.

Accordingly, the invention disclosed herein solves the foregoing difficulty by adopting the following configuration:

One invention disclosed herein comprises: a filmy resinous substrate; a resinous layer formed on a surface of said resinous substrate; and thin-film transistors formed on said resinous layer.

A specific example of the above-described configuration is shown in Fig. 1. In the configuration shown in Fig. 1, a resinous layer 102 is in contact with a PET film 101 having a thickness of 100 μm, the PET film being a filmy resinous substrate. Inverted-staggered thin-film transistors are formed on the resinous layer.

The material of the filmy resinous substrate can be selected from PET (polyethylene terephthalate), PEN (polyethylene naphthalate), PES (polyethylene sulfite), and polyimide. The requirements are flexibility and transparency. Preferably, the maximum temperature that the material can withstand is made as high as possible. If the heating temperature is elevated above 200°C, oligomers (polymers having diameters of about 1 μm) are generally deposited on the surface, or gases are produced. Therefore, it is quite difficult to form a semiconductor layer on the resinous substrate. Consequently, the material should have the highest possible processing temperature.

In the above-described structure, the resinous layer acts to planarize the surface of the resinous substrate. The planarization also serves to prevent precipitation of oligomers on the surface of the resinous substrate during steps involving heating such as the step for forming the semiconductor layer.

The material of this resinous layer can be selected from methyl esters of acrylic acid, ethyl esters of acrylic acid, butyl esters of acrylic acid, and 2-ethylhexyl esters of acrylic acid. Even if resinous substrates are used, this resinous layer can suppress the drawbacks with fabrication

of the afore-mentioned thin-film transistors.

The configuration of another invention comprises the steps of: forming a resinous layer on a filmy resinous substrate; forming a semiconductor layer on said resinous layer by plasma-assisted CVD; and forming thin-film transistors, using said semiconductor layer.

The configuration of a further invention comprises the steps of: heat-treating a filmy resinous substrate at a given temperature to degas said resinous substrate; forming a resinous layer on the filmy resinous substrate; forming a semiconductor layer on said resinous substrate by plasma-assisted CVD; and forming thin-film transistors, using said semiconductor layer.

In the above-described structure, heat-treatment is made to degas the resinous substrate, in order to prevent escape of gases from the resinous substrate during later processes involving heating. For example, if gases are released from the resinous substrate when a semiconductor thin film is being formed on the resinous substrate, then large pinholes are formed in the semiconductor thin film. This greatly impairs the electrical characteristics. Accordingly, the substrate is heat-treated at a temperature higher than heating temperatures used in the later processes, to degas the resinous substrate. In this way, release of gases from the resinous substrate during the later steps can be suppressed.

The configuration of a yet other invention comprises the steps of: heat-treating a filmy resinous substrate at a given temperature; forming a resinous layer on said filmy resinous substrate; forming a semiconductor layer on said resinous substrate by plasma-assisted CVD while heating the substrate to a temperature lower than said given temperature; and forming thin-film transistors, using said

semiconductor layer.

The configuration of a still other invention comprises the steps of: heat-treating a filmy resinous substrate at a given temperature which is higher than any heat-treatment temperature used in other steps; forming a resinous layer on said filmy resinous substrate; forming a semiconductor layer on said resinous substrate by plasma-assisted CVD; and forming thin-film transistors, using said semiconductor layer.

The configuration of a still further invention comprises: a pair of filmy resinous substrates; a liquid crystal material held between said resinous substrates; pixel electrodes formed on a surface of at least one of said resinous substrates; thin-film transistors connected with said pixel electrodes and formed on said resinous substrate; and resinous layers formed on surfaces of said filmy resinous substrates to planarize the surfaces.

A specific example of the above-described structure is shown in Fig. 3. In the structure shown in Fig. 3, a pair of resinous substrates 301, 302, a liquid crystal material 309 held between these resinous substrates, pixel electrodes 306, thin-film transistors (TFTs) 305 connected with the pixel electrodes 306, and a resinous layer 303 for planarizing the surface of the resinous substrate 301.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(A) to 1(E) are views illustrating a process sequence for fabricating thin-film transistors according to the present invention;

Figs. 2(A) to 2(C) are views illustrating another process sequence for fabricating thin-film transistors according to the present invention; and

Fig. 3 is a schematic cross-sectional view of a liquid

crystal panel.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

EXAMPLE 1

The present example shows an example in which inverted-staggered TFTs are formed on a substrate of PET (polyethylene terephthalate) which is an organic resin.

As shown in Fig. 1(A), a PET film 101 having a thickness of 100 μm is first prepared and heat-treated to degas the film. This heat-treatment is required to be conducted at a temperature higher than the highest temperature applied in later processes. In the processes shown in the present example, a temperature of 160°C used during formation of an amorphous silicon film by plasma-assisted CVD is the highest heating temperature. Therefore, the heat-treatment for degassing the PET film is performed at 180°C.

A layer of an acrylic resin 102 is formed on this PET film 101. As an example, a methyl ester of acrylic acid can be used as the acrylic resin. This acrylic resin layer 102 acts to prevent precipitation of oligomers on the surface of the PET film 101 in processes conducted later. The acrylic resin layer 102 also serves to planarize the uneven surface of the PET film 102. Generally, PET film surface has unevenness of the order of several hundreds of angstroms to 1 μm. Such unevenness greatly affects the electrical properties of the semiconductor layer having a thickness of several hundreds of angstroms. Therefore, it is quite important to planarize the base on which the semiconductor layer is formed.

Then, gate electrodes 103 of aluminum are formed. The gate electrodes 103 are formed by forming an aluminum film to a thickness of 2000 to 5000 Å (3000 Å in this example) by sputtering and performing a well-known patterning step

making use of photolithography. The gate electrodes 103 are etched so that the side surfaces are tapered (Fig. 1(A)).

Thereafter, a silicon oxide film acting as a gate-insulating film 104 is formed to a thickness of 1000 Å by sputtering. The gate-insulating film 104 may be made from silicon nitride instead of silicon oxide.

Subsequently, a substantially intrinsic (I-type) amorphous silicon film 105 is formed to a thickness of 500 Å by plasma-assisted CVD under the following conditions:

film formation temperature (at which the substrate is heated):	160°C
reaction pressure:	0.5 torr
RF power (13.56 MHz):	20 mW/cm^2
reactant gas:	SiH_4

In this example, the film is formed, using a parallel-plate plasma-CVD machine. The substrate is heated by a heater disposed within a substrate stage in which the resinous substrate is placed. In this way, the state shown in Fig. 1(B) is obtained.

Then, a silicon oxide film which acts as an etch stopper in a later step is formed by sputtering and then patterned to form an etch stopper 106.

Thereafter, an n-type amorphous silicon film 107 is formed to a thickness of 300 Å by parallel-plate plasma-assisted CVD under the following conditions:

film formation temperature (at which the substrate is heated):	160°C
reaction pressure:	0.5 torr
RF power (13.56 MHz):	20 mW/cm^2
reactant gases:	B_2H_6/SiH_4 = 1/100

In this way, the state shown in Fig. 1(C) is obtained.

Then, the n-type amorphous silicon film 107 and the substantially intrinsic (I-type) amorphous silicon film 105 are patterned by a dry-etching process. An aluminum film is formed to a thickness of 3000 Å by sputtering techniques. Thereafter, this aluminum film and the underlying n-type amorphous silicon film 107 are etched to form source electrodes 108 and drain electrodes 109. During this etching process, the action of the etch stopper 106 assures that the source and drain regions are isolated from each other (Fig. 1(D)).

An interlayer dielectric layer 110 is formed out of a resinous material such as silicon oxide or polyimide to a thickness of 6000 Å. Where a silicon oxide film is formed, a liquid which is applied when the silicon oxide film is formed may be used. Finally, contact holes are formed, and pixel electrodes 111 are fabricated from ITO. In this way, thin-film transistors arranged at the pixel electrodes of the active matrix liquid crystal display can be fabricated, using the transparent resinous substrate (Fig. 1(E)).

EXAMPLE 2

The present example shows a case in which an active matrix liquid crystal display is fabricated, using the thin-film transistors described in Example 1. The liquid crystal electrooptical device described in the present example is shown in Fig. 3 in cross section.

In Fig. 3, PET films 301 and 302 having a thickness of 100 μm form a pair of substrates. An acrylic resin layer 303 acts as a planarizing layer. Indicated by 306 are pixel electrodes. In Fig. 3, only the structure corresponding to two pixels is shown.

Indicated by 304 is a counter electrode. Orientation films 307 and 308 orient a liquid crystal 309 which can be a

twisted-nematic (TN) liquid crystal, supertwisted-nematic (STN) liquid crystal, or a ferroelectric liquid crystal. Generally, a TN liquid crystal is employed. The thickness of the liquid crystal layer is several micrometers to about 10 μm.

Thin-film transistors (TFTs) 305 are connected with the pixel electrodes 306. Electric charge going in and out of the pixel electrodes 306 is controlled by the TFTs 305. In this example, only one of the pixel electrodes 306 is shown as a typical one but a required number of other configurations of similar structure are also formed.

In the structure shown in Fig. 3, the substrates 301 and 302 have flexibility and so the whole liquid crystal panel can be made flexible.

EXAMPLE 3

The present example shows an example in which coplanar thin-film transistors used for an active matrix liquid crystal display are fabricated. The process sequence for fabricating the thin-film transistors of the present example is shown in Fig. 2. First, a PET film 201 having a thickness of 100 μm is prepared as a filmy organic resin substrate. The film is heated-treated at 180°C to promote degassing from the PET film 201. A layer of an acrylic resin 202 is formed on the surface of the film. In this example, an ethyl ester of acrylic acid is used as the acrylic resin.

Then, a substantially intrinsic (I-type) semiconductor layer 203 in which a channel formation region is formed is grown by plasma-assisted CVD under the following conditions:

film formation temperature
(at which the substrate is heated): 160°C

reaction pressure:	0.5 torr
RF power (13.56 MHz):	20 mW/cm^2
reactant gas:	SiH_4

In this example, a parallel-plate plasma-CVD machine is used to grow the film.

Then, an n-type amorphous silicon film is grown to a thickness of 300 Å by the parallel-plate plasma-CVD machine under the following conditions:

film formation temperature (at which the substrate is heated):	160°C
reaction pressure:	0.5 torr
RF power (13.56 MHz):	20 mW/cm^2
reactant gases:	B_2H_6/SiH_4 = 1/100

The n-type amorphous silicon film is patterned to form source regions 205 and drain regions 204 (Fig. 2(A)).

A silicon oxide film or silicon nitride film acting as a gate-insulating film is formed by sputtering techniques and patterned to form the gate-insulating film 206. Gate electrodes 207 are then formed from aluminum (Fig. 2(B)).

A polyimide layer 208 is formed as an interlayer dielectric film to a thickness of 5000 Å. Contact holes are formed. ITO electrodes 209 becoming pixel electrodes are formed by sputtering, thus completing TFTs (Fig. 2(C)).

EXAMPLE 4

The present example is similar to the structure of Example 1 or 2 except that the semiconductor layer is made of a microcrystalline semiconductor film. First, a substantially intrinsic semiconductor layer is grown as the microcrystalline semiconductor layer under the following conditions:

film formation temperature (at which the substrate is heated):	160°C
reaction pressure:	0.5 torr
RF power (13.56 MHz):	150 mW/cm^2
reactant gases:	SiH_4/H_2 = 1/30

In this example, a parallel-plate plasma-CVD machine is used to grow the film.

The conditions under which an n-type microcrystalline silicon film is grown are described below. Also in this case, a parallel-plate plasma-CVD machine is used.

film formation temperature (at which the substrate is heated):	160°C
reaction pressure:	0.5 torr
RF power (13.56 MHz):	150 mW/cm^2
reactant gases:	B_2H_6/SiH_4 = 1/100

Generally, a microcrystalline silicon film can be obtained by supplying power of 100 to 200 mW/cm^2. In the case of the I-type semiconductor layer, desirable results are obtained by diluting silane with hydrogen by a factor of about 10 to 50, as well as by increasing the power. However, if the hydrogen dilution is made, the film growth rate drops.

EXAMPLE 5

The present example relates to a method consisting of irradiating a silicon film with laser light having such a power that the filmy base or substrate is not heated, the silicon film having been formed by plasma-assisted CVD as described in the other examples.

A technique for changing an amorphous silicon film formed on a glass substrate into a crystalline silicon film by irradiating the amorphous film with laser light (e.g., KrF excimer laser light) is known. In another known technique, impurity ions for imparting one conductivity type are implanted into the silicon film and then the silicon film is irradiated with laser light to activate the silicon film and the impurity ions. The implantation of the impurity ions amorphizes the silicon film.

The configuration described in the present example makes use of a laser irradiation process as described above, and is characterized in that the amorphous silicon film 105 shown in Fig. 1 or the amorphous silicon films 203 and 204 shown in Fig. 2 are irradiated with quite weak laser light to crystallize the amorphous silicon film. If the previously formed film is a microcrystalline silicon film, the crystallinity can be improved.

KrF excimer laser or XeCl excimer laser can be used to emit the laser light. The energy of the emitted laser light is 10 to 50 mJ/cm^2. It is important that the resinous substrate 101 or 102 be not thermally damaged.

By utilizing the invention disclosed herein, the thickness of an active matrix liquid crystal display can be reduced. Also, the weight can be decreased. If an external force is applied, the substrates do not break. Flexibility can be imparted to the display.

This liquid crystal display can find wide application and is quite useful.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a filmy resinous substrate;

a resinous layer provided on said filmy resinous substrate; and

a semiconductor layer comprising silicon provided over said resinous layer.

2. The device of claim 1 wherein said semiconductor layer constitutes an inverted-staggered thin-film transistor.

3. The device of claim 1 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

4. The device of claim 1 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, 2-ethylhexyl ester of acrylic acid.

5. A semiconductor device comprising:

a filmy resinous substrate;

a resinous layer provided on said filmy resinous substrate; and

a thin film transistor comprising a semiconductor layer comprising silicon on said resinous layer;

an interlayer dielectric layer comprising a resinous material provided over said semiconductor layer; and

an indium tin oxide layer provided on said interlayer dielectric layer.

6. The device of claim 5 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

7. The device of claim 5 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, 2-ethylhexyl ester of acrylic acid.

8. The device of claim 5 wherein said interlayer dielectric layer comprises polyimide.

9. A semiconductor device comprising:

a filmy resinous substrate;

a resinous layer provided on said filmy resinous substrate; and

a semiconductor layer comprising silicon provided over said resinous layer,

wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

10. The device of claim 9 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, 2-ethylhexyl ester of acrylic acid.

ABSTRACT

A pair of substrates forming the active matrix liquid crystal display are fabricated from resinous substrates having transparency and flexibility. A thin-film transistor has a semiconductor film formed on a resinous layer formed on one resinous substrate. The resinous layer is formed to prevent generation of oligomers on the surface of the resinous substrate during formation of the film and to planarize the surface of the resinous substrate.

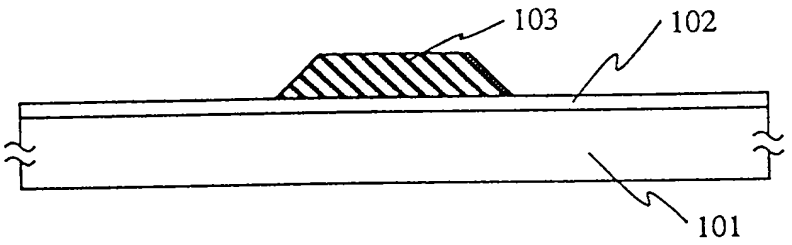

Fig. 1(A)

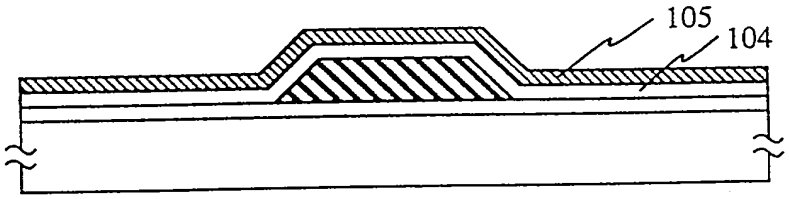

Fig. 1(B)

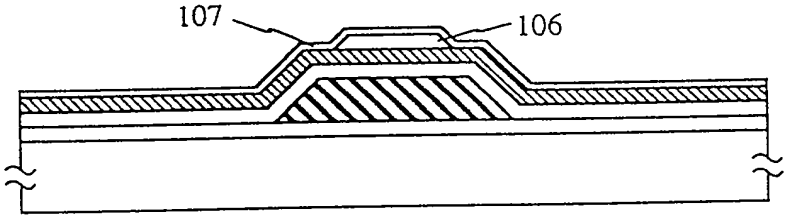

Fig. 1(C)

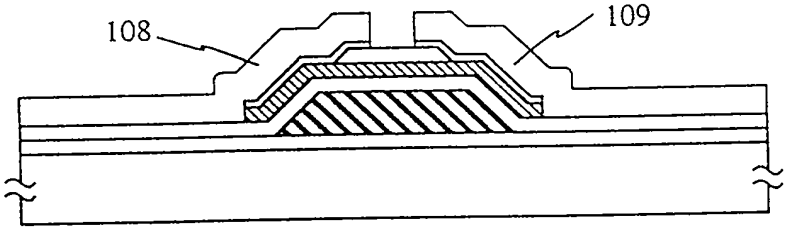

Fig. 1(D)

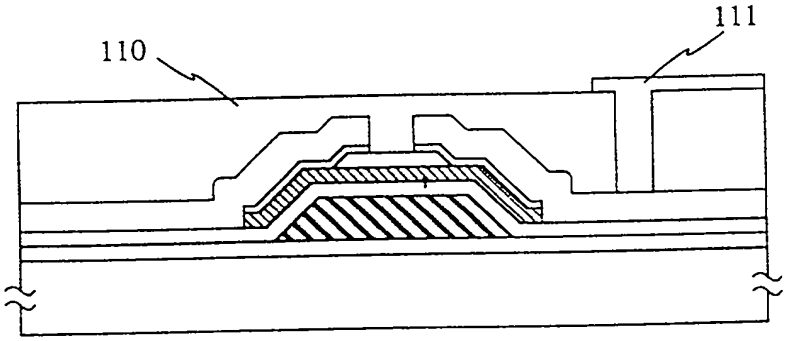

Fig. 1(E)

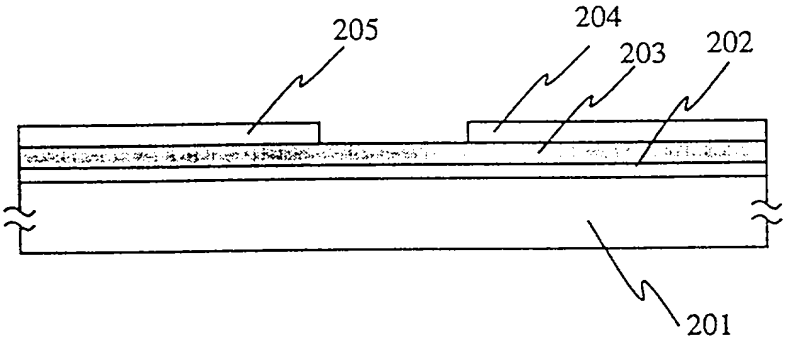

Fig. 2(A)

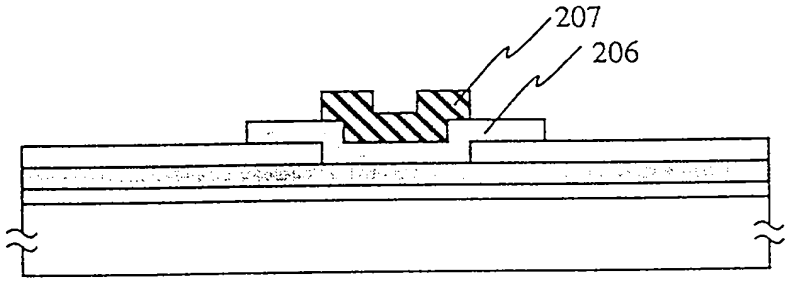

Fig. 2(B)

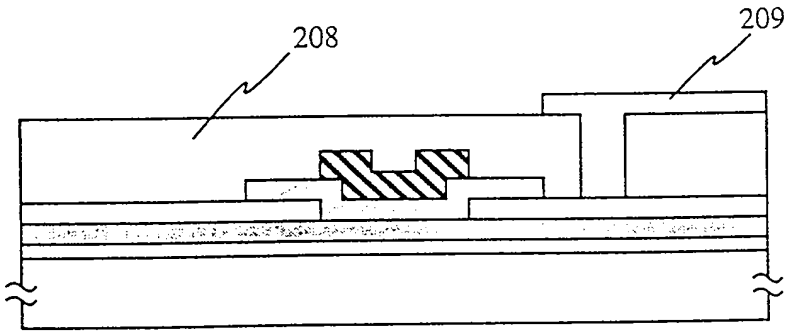

Fig. 2(c)

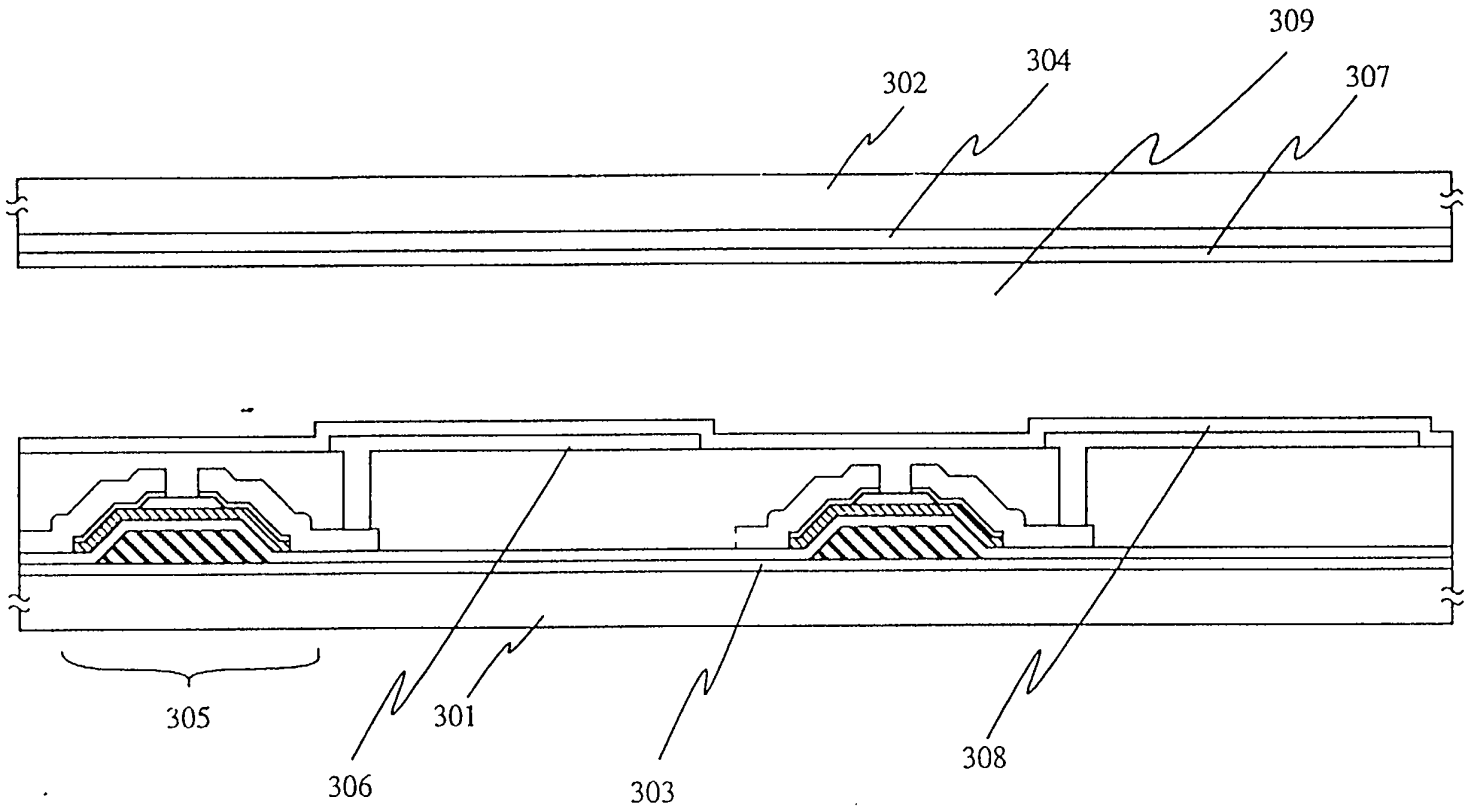

Fig. 3

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 0756-1464

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * Semiconductor Device, Method of Fabricating Same, and, Electrooptical Device

Insert Title

, the specification of which is attached hereto unless the following box is checked:

Check Box If Appropriate — For Use Without Specification Attached

☒ The specification was filed on December 20, 1995
and was assigned Serial No. 08/575,355 (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Priority Claimed

Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
6-339162	JAPAN	12/27/1994	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

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Stuart J. Friedman (Reg. No. 24,312)	David S. Safran (Reg. No. 27,997)
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed

Insert Residence Insert Citizenship

Insert Post Office Address

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